7.4 A 16Mb MRAM with FORK Wiring Scheme and Burst Modes

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MRAM is expected to become a universal memory solution, because it features non-volatility, unlimited writing cycles, and fast random-access speed. Previously presented MRAMs [1, 2], however, seem rather experimental, due to the small capacity, high power-supply voltage, and simple I/O interface. Considering that MRAM is suitable for mobile applications, a 16Mb MRAM compatible with asynchronous/synchronous pseudo SRAMs is designed and fabricated to target a commercial product.

To implement an 8-word page mode and 100MHz burst mode, compatible with that of 16-I/O asynchronous/synchronous pseudo SRAM, the read-out system is designed to have the 2-stage configuration that consists of a 128b simultaneous read-out stage and a parallel-serial conversion stage. As shown in Fig. 7.4.1, 8 cell arrays are activated in read cycle and 16 cells are accessed in each array, resulting in 8 words by 16 I/Os. The 128b data is latched into page buffers and then sequentially outputted by address inputs for page mode or the clock input for burst modes.

As shown in Fig. 7.4.2(a), 128 reference current generators that consume silicon area and power are needed to apply a conventional symmetric current-sensing scheme for the 128b simultaneous read-out. On the other hand, just one reference voltage is enough in voltage-sensing scheme. By converting the current mode into the voltage mode at the input node of the sense amplifier, the 128 sense amplifiers can be operated with just one voltage reference, as shown in Fig. 7.4.2(b). This single-reference scheme has another important advantage. In the conventional scheme, the reference current is generated by averaging the read-out current of paired '0' and '1' written reference cells that are connected with same RWL of the selected cell [1, 2]. Figure 7.4.3(a) shows the distributions of the measured resistance value of data '0', data '1', and reference cells (each being the average value of paired '0' and '1' written reference cells) from the sampling data of 32 rows × (32 + 2) columns on a test chip. It is known that reference-currents deviation cannot be avoided. Therefore, the single-reference scheme has wider sensing margin if properly designed.

A large parasitic capacitance in the read current path impedes to realize a fast access memory. With no additional metal layers, BL is separated into read BL (RBL) and write BL (WBL), that correspond to common-source node and read/write BL in the conventional cell, respectively, as shown in Figure 7.4.4(a). In read mode, the read-out current flows from a current conveyor to the grounded WBL by the WBL current driver, through the selected RBL, switch MOSs and magnetic tunnel junction (MTJ). And this BL configuration is suitable for FORK wiring scheme as mentioned in the next section.

Every MRAM developed so far, including the toggle MRAM [2], use magnetic field generated by WWL and WBL currents for writing. Because the sum of voltage drops caused by WWL or WBL wiring resistances and write current driver MOSs cannot exceed the power supply voltage, the wiring resistance imposes a serious restriction on WWL/WBL length and on the memory array size. Small cell arrays with write current drivers and sense amplifiers make the chip size larger and raise the chip cost. Reducing the write currents and/or the wiring resistances are key design issues for MRAM scaling. A special shape MTJ, shown in Figure 7.4.4(b), is applied to reduce the writing currents [3]. FORK-wiring scheme, shown in Figure 7.4.5, is also implemented in order to reduce the wiring resistances.

For selective writing by the combined magnetic-field generated by WWL and WBL currents, the currents must flow in the vicinity of the target MTJ. Except for the vicinity, the current can be flown in any distributed paths. For example, on 4 tine FORK scheme, shown in Figure 7.4.5(b), 4 wires are connected at the center of the wires. By controlling the write current drivers, 4 currents are divided from the connection point after flowing in the vicinity of the target MTJ just like a fork shape, not affected to the selectivity. The wiring resistance can be reduced to (1+1/4)/2=5/8 as compared with the conventional scheme. A cell array size can be made larger, from 256 rows × 256 columns to 512 rows × 512 columns and the number of cell arrays reduced from 256 to 64 in the restriction of 1.8V power supply. Because of the area reduction of current drivers and sense amplifiers, the cell efficiency is raised from 27.1% to 39.9%, as shown in Fig. 7.4.6. The chip size is reduced from 115.96mm^2 to 78.74mm^2.

On the other hand, the number of the half-selected MTJs, which has raised the probability of data inversion by thermal fluctuation, gets larger than that of a conventional scheme. For the half-selected MTJs in the tine area, the half-selected cycles multiply by 4 times, but the magnetic field is reduced to 1/4. Therefore, the probability ratio of thermal fluctuation is reduced by $1/4 \times \exp(-K_uV/k_BT \times [(1-H_s/4H_k)^2-(1-H_s/H_k)^2]) < 1$, from the formula (10) in the reference [4], where K_u, V, H_s, and H_k are the anisotropic energy, volume, switching and anisotropic magnetic field of the storage layer of the MTJ, respectively. Therefore, FORK wiring scheme has not only raised the memory cell efficiency but also raised the reliability for non-volatile memory. While the combined resistance can be reduced by adopting the larger tine number, the replacement unit of redundancy gets larger and less efficient. In this work, 4 is selected.

Latency and burst length can be set by internal registers. Figure 7.4.7 shows the simulation waveform of the burst-read mode when read latency and burst length are 4 clocks and 16, respectively. The 34ns address access time and 100MHz burst-mode frequency meet the specifications of standard asynchronous/synchronous pseudo SRAM. The 10.2 × 7.72mm^2 16Mb MRAM is realized in 4M 0.13μm 1.8V CMOS technology using the 1.44 × 1.3μm^2 memory cell.

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[4] M. P. Sharrock, "Time Dependence of Switching Fields in Magnetic Recording Media," J. Appl. Phys., vol. 76, no. 10, pp. 6413-6418, Nov., 1994.

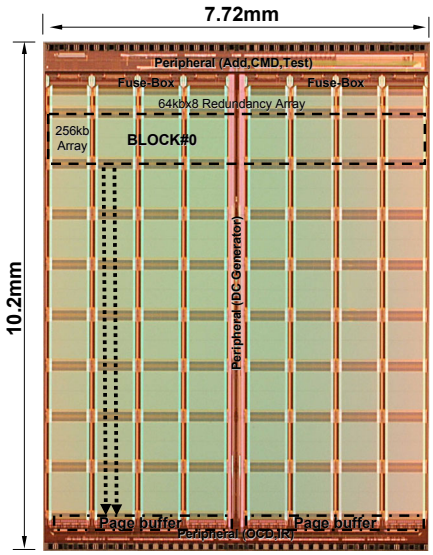

Figure 7.4.1: Chip micrograph.

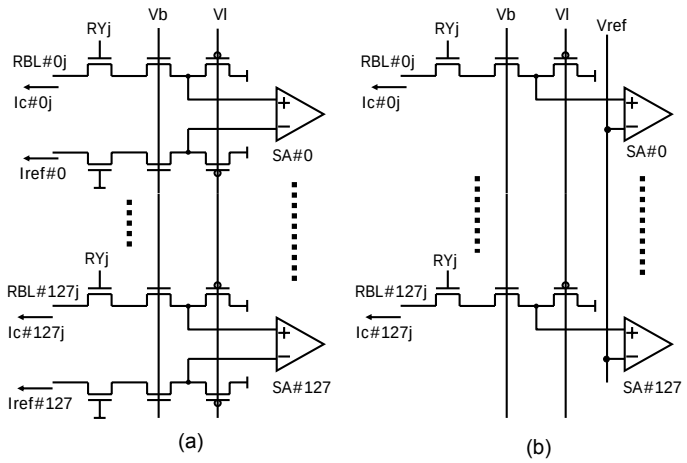

Figure 7.4.2: Reference scheme, (a) symmetric current reference,(b) single voltage reference.

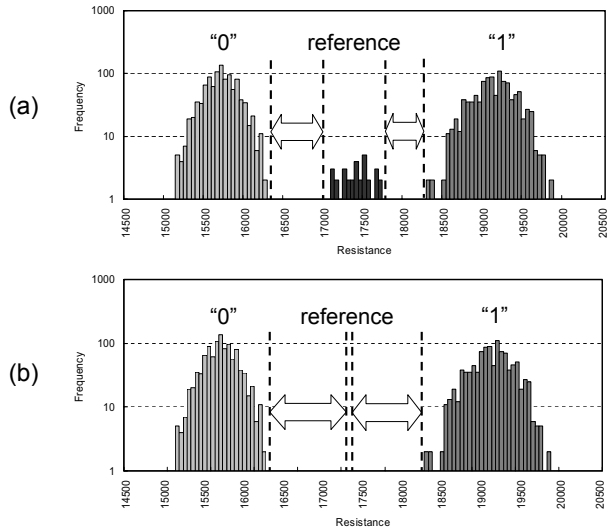

Figure 7.4.3: Resistance distribution, (a) paired reference cells par WL, (b) single reference.

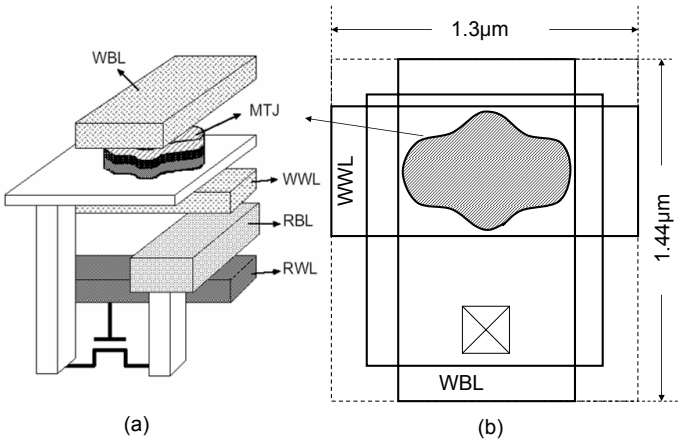

Figure 7.4.4: Memory cell, (a) bird's-eye view, (b) plain view.

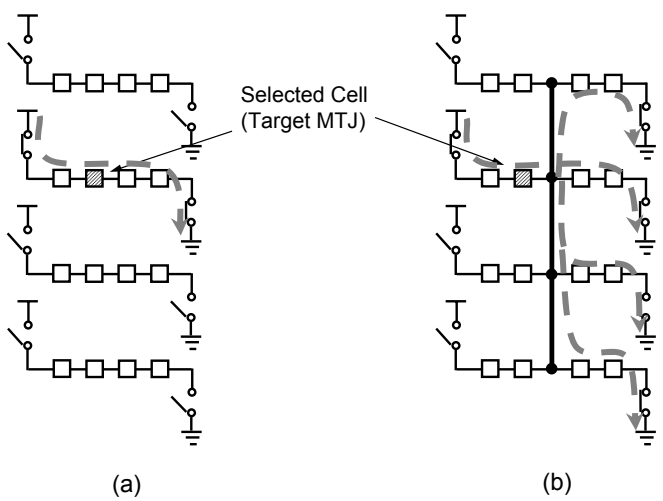

Figure 7.4.5: Write current flow, (a) conventional, (b) 4 tine FORK.

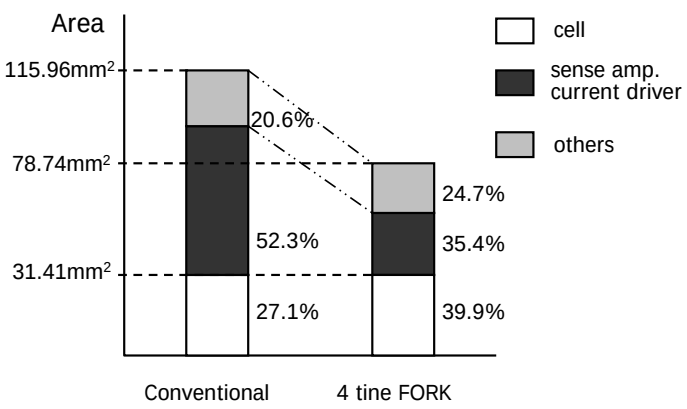

Figure 7.4.6: Chip size and cell efficiency.

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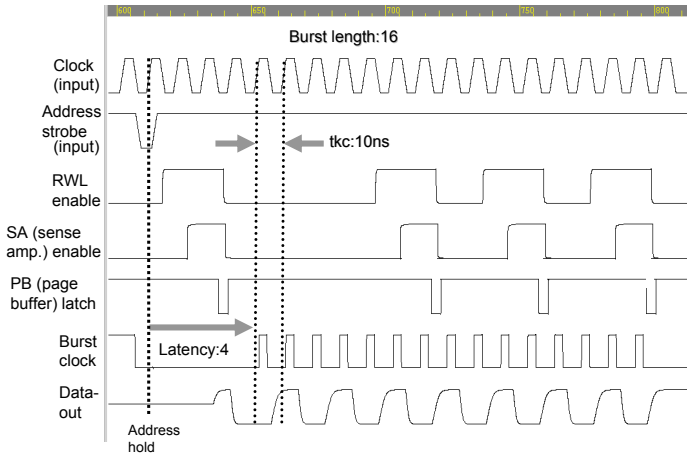

Figure 7.4.7: Simulation waveform of the burst-read mode.

